**IN THE SPECIFICATION**

Please replace the entire paragraph on page 1, lines 16-18, of the specification, with the following.

**1. Field of the Invention**

The present invention relates in general to the field of ~~analog/digital~~ analog-to-digital conversion circuits or converters (ADCs).

Please replace the entire paragraph on page 1, line 20 to page 2, line 5, of the specification, with the following.

**2. Description of the Related Art**

~~Analog-To-Digital~~ Analog-to-digital ~~(ADC) converters~~ converters (ADCs) are commonly used in several applications (for example, in the telecommunication field), whenever an analog input signal is to be converted into a corresponding digital output signal. The basic component of every converter is a quantizer. The quantizer compares an analog signal with one or more predefined threshold values; the combination of the results of the comparisons uniquely identifies the digital representation of the analog signal. In order to achieve a high resolution of the whole converter, quantizers of the parallel type are commonly used; in this case, the analog signal is compared with multiple threshold values at the same time.

Please replace the entire paragraph on page 3, line 23 to page 4, line 2, of the specification, with the following.

This drawback is particular acute in applications working with wide-band signals and requiring high resolutions (for example, in modern mobile telecommunication techniques such as the UMTS). In this case, a commonplace solution is that of using a ~~sigma-delta~~ sigma-delta ($\Sigma\Delta$), or ~~delta-sigma, ($\Sigma\Delta$)~~ delta-sigma ($\Delta\Sigma$) architecture.

Please replace the entire paragraph on page 4, line 22 to page 5, line 6, of the specification, with the following.

The number of filters in the sigma-delta converter defines the degree of noise-shaping (referred to as the order of the sigma-delta converter). Sigma-delta converters with a single-loop structure are typically designed with an order of one or two because of instability problems. Whenever a higher order is required, a multistage architecture implementing two or more loops is commonly used. A multistage architecture including at least one sigma-delta converter, also known as MASH (MultistAge noise SHaping), is inherently stable; moreover, a MASH converter provides performance comparable to the one of a single-loop ~~convert~~ converter having an order equal to the sum of the orders of the different stages of the MASH converter.

Please replace the entire paragraph on page 7, lines 6-14, of the specification, with the following.

The converter 100 has a multistage architecture, with a plurality of cascade-connected stages. In the example shown in the ~~figure~~ Figure 1, the converter 100 includes a first stage 105 consisting of a sigma-delta converter of the second order; the sigma-delta stage 105 is followed by a stage 110 of the pipeline type. The above-described structure defines a MASH architecture. A MASH converter is commonly designated adding, for each stage, a number denoting the order of the stage (the number is set to 0 for a stage that is not of the sigma-delta type); therefore, the converter 100 at issue will be denoted with $MASH_{20}$.

Please replace the entire paragraph on page 8, lines 1-13, of the specification, with the following.

The digital output signal $Y_2(z)$ is applied to a ~~Digital-To-Analog~~ digital-to-analog (DAC) converter 120. The DAC 120 re-converts the digital output signal $Y_2(z)$ into a corresponding analog signal. An adder 125a subtracts the analog output signal $Y_2(z)$ from the analog input signal X(z). The resulting analog delta signal is provided to a filter 130a. The filter 130a integrates the analog delta signal and shapes the quantization error according to a transfer function $H_a(z)$ of the filter 130a. A further adder 125b subtracts the analog output signal $Y_2(z)$ from the analog signal provided by the filter 130a. The resulting analog delta signal is applied to a further filter 130b, which performs

an additional noise shaping process based on its transfer function $H_b(z)$. Therefore, the filter 130b provides an analog signal $V_2(z)$ that is shaped according to the transfer functions $H_a(z)$ and $H_b(z)$; this analog shaped signal $V_2(z)$ is then supplied to the flash ADC 115, which delivers the digital output signal $Y_2(z)$.

Please replace the entire paragraph on page 13, lines 10-14, of the specification, with the following.

However, the concepts of the present invention are also applicable when the logic module has another structure or includes equivalent components; similar considerations apply if the decimation parameter of the ~~sinc~~ sync filter has a different value, if the digital signals have another resolution, and the like.

Please replace the entire paragraph on page 19, line 23 to page 20, line 3, of the specification, with the following.

This additional feature avoids the need of using a servo-DAC that is very accurate and expensive. Moreover, it increases the stability of the whole converter. The corresponding loss of resolution does not substantially affect the effectiveness of the algorithm; in fact, the solution of the invention does not require a very high accuracy (being enough to ensure that the analog correction signal avoids the overflow of the next stages).

Please replace the entire paragraph on page 20, lines 5-11, of the specification, with the following.

Alternatively, the digital correction signal is calculated only from the digital signal output by the stage directly following the selected one (thereby reducing the resolution of the digital correction signal but avoiding the addition of the offset errors of the ~~other~~ next stages); moreover, the solution of the present invention leads itself to be implemented even with a different resolution of the stages following the selected one, or without reducing the resolution of the digital correction signal.

Please replace the entire paragraph on page 20, lines 19-20, of the specification, with the following.

A suggested choice for calculating the digital correction signal is to use a ~~sinc~~ sync filter followed by an integrator.

Please replace the entire paragraph on page 20, lines 22-24, of the specification, with the following.

The proposed structure ensures the convergence of the algorithm; moreover, the decimation parameter of the ~~sinc~~ sync filter makes it possible to control either the precision or the convergence speed of the process.